Introduction to Digital Logic

EECS/CSE 31L

**Assignment 4 Design Report**

**Designing Register File**

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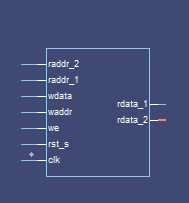
1 BLOCK Description

This 32-bit Register File is a single-port register file that supports two read and one write at each clock cycle. This register file only has a synchronous reset and does not have an asynchronous reset, meaning the only way to reset the data is when there is a rising a clock edge. Every time the rising clock edge appears, it will read two addresses the user inputs and writes a 32-bit into the address the user inputs.

2 Input/Output Port Description

|  |  |  |  |
| --- | --- | --- | --- |
| Port Name | Port Size | Port Type | Description |
| clk | 1 | IN | The Clock Cycle |
| rst\_s | 1 | IN | Synchronous Reset Signal (1 = Reset) |
| we | 1 | IN | Write Enable Signal |
| raddr\_1 | 3 | IN | 1st Read Address Signal |
| raddr\_2 | 3 | IN | 2nd Read Address Signal |
| waddr | 3 | IN | Write Address Signal |
| rdata\_1 | 32 | OUT | 1st Read Data Signal |
| rdata\_2 | 32 | OUT | 2nd Read Data Signal |
| wdata | 32 | IN | Write Data Signal |

3 Design Schematic



4 Wave

